This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A method for implementing at speed bit fail mapping of an embedded memory system having a BIST (Built In Self Testing) engine, comprising:

using a high speed multiplied clock which is an asynchronous multiple of [[an]] a slower external clock of a tester to sequence BIST bit fail testing of the embedded memory system, said BIST generating a fail map data including all diagnostic fails for capture by a diagnostic register device under control of said high speed multiplied clock, the diagnostic fail data being stored in fail location latches of said diagnostic register device at a time of recognizing said BIST fail test;

generating a signal for receipt by said tester to identify a BIST bit fail test for said tester, and;

in response to said generated signal, implementing a BIST clock control logic for automatically pausing the BIST bit fail testing upon recognition of a fail of the embedded memory system, said BIST clock control logic gating off said high speed multiplied clock to BIST test latches and fail location latches of said diagnostic register;

receiving, from said tester, a first signal asserted in response to receiving said generated signal;

said BIST clock control logic automatically switching, in response to said received asserted first signal, ~~reconfiguring~~ said diagnostic register device to operate from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the slower external clock of the tester;

using the slower external clock of the tester to read bit fail data out from said fail location latches of said diagnostic register device to the tester; and,

receiving, from said tester, a de-asserted first signal when all fail data out from said fail location latches of said diagnostic register device are read;

automatically switching, in response to said received de-asserted first signal, said BIST clock control logic to resume data capture at said fail location latches of said diagnostic register device at said high speed multiplied clock; and,

resuming the BIST testing with the high speed multiplied clock from the point at which it was paused, wherein diagnostic bit fail data is extracted from said diagnostic register device without disturbing a state of said BIST or said embedded memory.

2. (Original) The method of claim 1, used for bit fail mapping of an embedded DRAM (Dynamic Random Access Memory).

3. (Original) The method of claim 2, including using an on-chip clock multiplier to multiply the external clock to generate the high speed multiplied clock.

4. (Previously Presented) The method of claim 3, including using the on-chip clock multiplier to multiply the external clock of an off-chip ATE (Automatic Test Equipment) tester to generate the high speed multiplied clock.

5. (Canceled)

6. (Currently Amended) The method of claim [[5]] 4, ~~further including using~~ wherein said BIST clock control logic includes a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the BIST clock control logic causes the multiplexer to pass either the first input from the tester clock for reading said read bit fail data out from said fail location latches of said diagnostic register device or the second input from the high speed multiplied clock during data capture.

7. – 12. (Canceled)

13. (Currently Amended) A circuit for implementing at speed bit fail mapping of an embedded memory system having a BIST (Built In Self Testing) engine on a chip, comprising:

an off-chip tester having a tester clock;

the BIST engine using a high speed multiplied clock which is an asynchronous multiple of the tester clock to sequence the BIST engine for bit fail testing of the embedded memory system, said BIST engine generating a fail map data for capture [[by]] at fail location latches of a diagnostic register device, the diagnostic fail data being stored in fail location latches at a time of recognizing said BIST fail test, and generating a signal for receipt by said off-chip tester to identify a BIST bit fail test for said tester;

the circuit including BIST clock control logic, responsive to said generated signal, for pausing the BIST testing upon recognition of a fail of the embedded memory system, said BIST clock control logic gating off said high speed multiplied clock to BIST test latches and fail location latches of said diagnostic register;

said off-chip tester asserting, for receipt by said circuit, a first signal in response to receiving said generated signal;

~~the circuit including~~ said BIST clock control logic for automatically switching, in response to said received asserted first signal, ~~reconfiguring~~ said diagnostic register device to operate from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the tester clock,

the circuit using the tester clock to read bit fail data out to the tester from said fail location latches of said diagnostic register device, and,

said off-chip tester de-asserting said first signal for receipt by said BIST clock control logic when all fail data out from said fail location latches of said diagnostic register device are read; and,

~~thereafter resuming the BIST testing with the~~ said circuit, in response to said received de-asserted first signal, to resume data capture at said fail location latches of said diagnostic register device at said high speed multiplied clock from the point at which BIST testing was paused, wherein diagnostic bit fail data is extracted from said diagnostic register device without disturbing a state of said BIST or said embedded memory.

14. (Original) The circuit of claim 13, for automatic bit fail mapping of an embedded DRAM (Dynamic Random Access Memory), including an on-chip clock multiplier for multiplying the tester clock of an off-chip ATE (Automatic Test Equipment) tester to produce the high speed multiplied clock, wherein the logic pauses the BIST engine at a point when a mismatch between BIST expected data and the actual data read from the DRAM is encountered, then shifts the bit

fail data off the chip using the low-speed ATE tester clock, and then resumes the BIST engine using the high speed multiplied clock to provide an at speed bit fail map.

15. (Canceled)

16. (Currently Amended) The circuit of claim [[15]] 14, further comprising a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the logic causes the multiplexer to pass either the first input from the tester clock or the second input from the high speed multiplied clock to the BIST engine.

17. – 20. (Canceled)

21. (Currently Amended) [[The]] A circuit ~~of claim 18,~~ for enabling at speed bit fail mapping of an embedded Dynamic Random Access Memory (DRAM) system, the circuit comprising:

a bit fail map data register having diagnostic latches used to store data on failing memory locations for the generation of a bit fail map in a data capture mode controlled by a high speed multiplied clock which is an asynchronous multiple of a slower tester clock, an on-chip clock multiplier provided for multiplying said slower tester clock of an off-chip ATE (Automatic Test Equipment) tester to produce said high speed multiplied clock;

a first control latch that asserts a pause signal upon receiving a fail data signal indicating a mismatch comparison between expected data from the embedded memory system and actual data read from the embedded memory system, the bit fail map data being stored in said diagnostic latches at a time of recognizing a BIST bit fail test;

a second control latch that is set upon receiving the pause signal from the first control latch and asserts a shift enable signal to enable a shift out of the data on failing memory locations from the bit fail map data register in a serial transfer mode controlled by the slower tester clock for the generation of a bit fail map, and,

logic which includes the first and second control latches operable to pause a BIST (Built In Self Testing) engine at a point when a mismatch between BIST expected data and the actual data read from the DRAM is encountered, said logic causing said shifting out the bit fail data off the bit fail map data register using the slower ATE tester clock, and then resuming the BIST engine using the high speed multiplied clock to provide an at speed bit fail map,

said pause signal of the first control latch pausing BIST engine test circuitry for testing the embedded memory system and enabling a continue/handshake signal from said off-chip ATE to enable the second control latch to assert the shift enable signal to enable a shift out of the data on failing memory locations from the bit fail map data register for the generation of a bit fail map,

wherein the bit fail map data register includes fail location latches for storing the location of the fail upon recognition of the fail, and the logic that ~~stops~~ pauses the BIST engine also de-gates [[a]] the slower ATE tester clock to the fail location registers, allowing the bit fail data to be shifted off the chip to the ATE tester at the slower ATE tester clock speed,

wherein the first and second control latches include both master latches, which are clocked with function data with a function clock or with scan data with a scan clock, and slave latches which are updated with master latch data with a slave latch clock,

wherein diagnostic bit fail data is extracted from said diagnostic register device without disturbing a state of said BIST or said embedded memory.

22. (Original) The circuit of claim 21, further comprising a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the logic causes the multiplexer to pass either the first input from the tester clock or the second input from the high speed multiplied clock to the BIST engine.

23. (Previously Presented) The method of claim 1, wherein new fail map data is captured on every high speed multiplied clock cycle.

24. (Canceled)

25. (Previously Presented) The circuit of claim 13, wherein new fail map data is captured on every high speed multiplied clock cycle.